REMARKS

The Examiner's comments and the cited art have been noted and carefully studied. Applicants respectfully traverse the rejections and request reconsideration. For the reasons set forth below, Applicants submit the claims are allowable as written. Applicants respectfully traverse and request reconsideration. Claims 1, 2, 4, 6-10, 12-16 and 18-22 are pending. Claim 22 is allowed.

Applicants wish to thank the Examiner for the indication that Claims 6, 7, 9, 12, 13, 19, 20 and 21 would be allowable if rewritten in independent form.

Independent Claim 1

Independent claim 1 recites, among other features, a single gate oxide differential receiver to receive a differential receiver supply voltage from a switchable voltage supply circuit. (Claim 1). The single gate oxide differential receiver functions as an input/output buffer that can operate at different voltage levels, such as 3.3 volts, or 1.5 volts. The input/output buffer functions as an I/O pad to interface with, for example, a CMOS graphics controller chip (core logic 18) operating at 2.5 volts, for example and with other processing chips operating at 3.3 volts or 1.5 volts via pad 16. (Specification, p 1, lines 25 – 27). The processing chips are required to work with for example, both, a 3.3 volt I/O voltage supply as well as with a 1.5 voltage supply. (Spec. p2, lines 22-24). (Spec. p2, lines 24-25). Accordingly, this typically means that the input signal received by the single gate oxide differential receiver can have a 0 Volt to 1.5 Volt swing for one application and a 0 to 3.3 Volt swing for another application. If the differential receiver is powered from a 3.3 volt supply voltage, then the differential receiver, based on for example thick gate oxide MOS transistors, will be too slow if powered with the 1.5 Volt supply. Conversely, if the differential receiver is powered from a 1.5 volt supply, then the differential receiver, based on for example, a thin gate oxide MOS transistors cannot typically withstand the 3.3 volt supply or the 3.3 volt input signal. The claimed single gate oxide differential receiver solves the problem of accommodating a varying supply voltage that automatically accommodates different supply voltages and input signal levels on a single integrated circuit chip. According to one embodiment, the switchable voltage supply circuit provides a 3.3 volt supply voltage to the differential receiver when the processing chips operate at 3.3 volts in order to provide required processing speed. Further, the switchable voltage supply

circuit provides a 2.5 volt supply voltage to the differential receiver when the processing chips operate with 1.5 volt input signals in order to provide the required processing speed. In this case, the differential receiver supply voltage, 2.5 volts, is higher than a maximum voltage level of the input voltage.

SETTY

Setty discloses a differential comparator circuit commonly used in high-speed analog to digital (A/D) converters. (Setty Col. 4, lines 26-29). Before amplification, Setty requires the differential amplifier enter into an "auto-zero" mode in order to compensate for any output offset.

> Referring to FIG. 2, **before differential amplifier 10 begins amplification**, switches S1 and S2 are closed and the inputs V_{IP} and V_{IM} are set at their common-mode voltage V_{CM}. Nodes V1 and V2 **charge to a common-mode voltage set by the output of differential amplifier** 10. In an offset-free differential amplifier, the voltages at nodes V1 and V2 are substantially equal to the output common-mode voltage of the differential amplifier. However, in the presence of the amplifier offset, the difference between the voltages on nodes V1 and V2 is substantially equal to the amplifier offset. This mode, where the offset and input common-mode of the amplifier and the reference common mode of the input signal are acquired and/or set, is commonly referred to as the "**auto-zero**" or "offset acquisition" mode.

(Setty, Col. 1, lines 41-54). (emphasis added). Accordingly, Setty requires entry into an auto-zero mode before the differential amplifier begins amplification.

CLAIM REJECTED UNDER 35 U.S.C. § 112

not what rejected in claim

Claim 2 is rejected under 35 U.S.C. 112, second paragraph as being indefinite "because the differential receiver supply voltage is a voltage at the I/O pad supply voltage" (Office Action June 18, 2003, Page 2 Ref. #2). There are two different voltages available to the switchable voltage supply circuit, one is the input/output pad supply voltage i.e. 1.5 volts as shown in Fig. 2, and the other is the differential receiver supply voltage i.e. 2.5v shown as V_{REF} 10 in Fig. 2. Since the differential receiver supply voltage i.e. 2.5 volts is greater than the input/output pad supply voltage i.e. 1.5 volts, then the differential receiver supply voltage is selected. However, if the differential receiver supply voltage, i.e. 2.5 volts is not greater than the input/output pad

supply voltage, i.e. 3.3 volts, then the input/output pad supply voltage, i.e. 3.3 volts is selected. As to Claim 2, Setty, as understood, does not "select[s] the differential receiver supply voltage that is a higher voltage than the I/O pad supply voltage." According to the Office Action dated 12/13/2002 on page 4, reference # 4, the input/output pad supply voltage corresponds to Vdd EXTERNAL terminal of Figure 3 in Setty. However, since Vdd INTERNAL in Setty is always less than Vdd EXTERNAL, Setty fails to teach, and teaches an approach opposite to "select[s] the differential receiver supply voltage that is a higher voltage than the I/O pad supply voltage." Consequently, claim 2 is not indefinite. Accordingly, for at least this reason, claim 2 is allowable.

CLAIM REJECTED UNDER 35 U.S.C. § 102(E)

Claim 1 stands rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,091,300 (Setty).

SETTY AS CITED FAILS TO RECITE "AT LEAST ONE OF THE SELECTED RECEIVER SUPPLY VOLTAGES IS HIGHER THAN A MAXIMUM VOLTAGE LEVEL OF THE INPUT VOLTAGE"

According to the Office Action, the auto-zero mode taught by Setty is irrelevant to the claim. Firstly, Setty teaches against "at least one of the selected receiver supply voltages is higher than a maximum voltage level of the input voltage" because Setty teaches that the supply voltage is dropped as a result of entering the "auto-zero" mode before differential amplifier begins amplification.[1]

> Assuming that the differential amplifier is configured as shown in FIG. 2 (with differential amplifier 20 replacing differential amplifier 10), **during the auto-zero mode** when switches S1 and S2 are closed, the output common-mode voltage of the differential amplifier 20 is changed by **dropping the supply voltage** thereto by a predetermined amount. This is symbolically shown by inserting a battery V.sub.A between the external supply voltage

[1] A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 U.S.P.Q. 303 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984), M.P.E.P. 2141.02.

> V.sub.DD and the sources of devices M5 and M6 as shown in FIG. 3. With this modification, during the auto-zero mode, the voltages at nodes V1 and V2 are equal to V.sub.DD -V.sub.A |.V.sub.GS|., where .|.V.sub.GS|.. is the absolute value of the gate-source voltage of transistors M5 and M6.

(Setty, Col. 3, lines 4-16). (emphasis added). Since Setty drops the supply voltage during the auto-zero mode, and the auto-zero mode is entered before amplification begins, Setty teaches an approach completely different from "wherein, at least one of the selected receiver supply voltages is higher than a maximum voltage level of the input voltage." Secondly, Setty is silent with respect to lowering the supply voltage based on any input voltage because Setty teaches an opposite approach, rather the dropping of the supply voltage for the "auto-zero" mode where the voltages at nodes V1 and V2 are equal to V_{DD}-V_A-1V_{GS}1 rather than wherein at least one of the selected receiver supply voltages is higher than the maximum voltage level of the input signal voltage. As a result, Setty fails to teach all the elements as arranged in claim 1. For any or all of the above reasons, Claim 1 is allowable.

CLAIM REJECTION UNDER 35 U.S.C. § 103(A)

Claims 4, 8, 10, 14-16 and 18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Setty. Firstly, Applicants respectfully reassert the relevant remarks made above with respect to Claim 1.

SETTY AT LEAST FAILS TO TEACH "WHEREIN THE SWITCHABLE VOLTAGE SUPPLY CIRCUIT SELECTS THE DIFFERENTIAL RECEIVER SUPPLY VOLTAGE FOR THE SINGLE GATE OXIDE DIFFERENTIAL RECEIVER TO BE A VOLTAGE LEVEL HIGHER THAN A MAXIMUM VOLTAGE LEVEL OF THE INPUT LINE.

As to claim 4, Setty at least fails to teach "wherein the switchable voltage supply circuit selects the differential receiver supply voltage for the single gate oxide differential receiver to be a voltage level higher than a maximum voltage level of the input line." By contrast, as stated above, Setty teaches that the supply voltage is dropped as a result of entering the "auto-zero" mode rather than "the switchable voltage supply circuit selects the differential receiver supply voltage for the single gate oxide differential receiver."

Secondly, rather than select the supply voltage based on "a maximum voltage level of the input line" as claimed, Setty, reacts when entering into "auto-zero" mode. Accordingly, Setty does not teach all the elements as arranged in the claim.

Thirdly, the Office Action acknowledges that Setty does not disclose a reference voltage on a first differential input and an input voltage on a second differential input. However, Setty teaches against "receives a reference voltage on a first differential input and an input voltage on a second differential input" because Setty teaches the incompatible approach of causing switches S1 and S2 to close during the "auto-zero" mode causing the inputs V_{IP} and V_{IM} to be set at their common-mode voltage V_{CM}. Since Setty requires that inputs V_{IP} and V_{IM} be set at their common-mode voltage V_{CM}, Setty teaches against, "a reference voltage on a first differential input and an input voltage on a second differential input."

Fourthly, rather than select the supply voltage as claimed, "to be a voltage level higher than a maximum voltage level of the input voltage", Setty merely sets the inputs to their common-mode voltage. When SA in Setty is open, the voltage at VDD-INTERNAL is VDD-VA, which as understood may be lower than the maximum voltage level of the input voltage, in contrast to the claims. Accordingly, Setty as cited does not teach "wherein the switchable voltage supply circuit selects the differential receiver supply voltage for the single gate oxide differential receiver to be a voltage level higher than a maximum voltage level of the input line."

Fifthly, Setty teaches against the claimed invention because the modifications suggested would change the principle of operation, i.e., (A/D converter). Setty's circuit would not function as an A/D circuit because as an input/output pad, the outputs Vom and Vop driven by M5 and M6 do not provide the appropriate range swing, i.e. negative or positive wing. For example, when the input signal at VIP and VIM is at a voltage corresponding to a logic 0, M1 and M2 would switch off thus preventing outputs VOM and VOP from providing a proper output voltage corresponding to a logic level.[2] Also, the single gate oxide gate of the claims can withstand the

[2] If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious. *In re Ratti*, 270 F.2d 810, 123 U.S.P.Q. 349 (CCPA 1959). *See* M.P.E.P. 2143.01.

selected supply voltages, whereas the circuit in Setty would fail because the gate to source and gate to drain maximum limits would be exceeded thus rendering the circuit in Setty inoperable.[3]

Claim 8 requires that the receiver of Claim 1 "generate an output signal to circuitry for a videographics processor." The Office Action asserts that such circuitry is seen in many applications. Hence, an output signal must be generated as well as suitable coupling to communicate the output signal to the circuitry for a videographics processor. Setty is silent as to any such structure. Pursuant to M.P.E.P.2149.03, Applicants traverse the assertion in the Office Action and request a cite to a supporting reference. Applicants further submit that this claim is also allowable in light of the presence of novel and non-obvious elements.

As to Claim 10, Applicants respectfully reassert at least the relevant remarks made above with respect to Claims 1 and 4. Applicants further submit that this claim is also allowable in light of the presence of novel and non-obvious elements.

As to Claim 18, Applicants respectfully reassert the relevant remarks made above with respect to Claim 1 and further note that Setty fails to recite an isolation output buffer as recited in the claim. Accordingly, this claim is also believed to be in condition for allowance. Applicants further submit that this claim is also allowable in light of the presence of novel and non-obvious elements.

As to Claims 14-16, Applicants respectfully reassert the relevant remarks made above with respect to at least claims 1, 4, 10, and 18. Applicants further submit that this claim is also allowable in light of the presence of novel and non-obvious elements.

Applicants respectfully submit that the claims are in condition for allowance and respectfully request that a timely Notice of Allowance be issued in this case. The Examiner is

---

[3] If the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 200, 221 U.S.P.Q. 1125 (Fed. Cir. 1984); M.P.E.P. 2143.02.

invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

By: _____
Themi Anagnos
Registration No. 47,388

Date: August 18, 2003

VEDDER, PRICE, KAUFMAN &
KAMMHOLZ, P.C.
222 N. LaSalle Street
Chicago, IL 60601
(312) 609-7599
FACSIMILE: (312) 609-5005